In the Claims:

Please cancel claims 40, 49, and 84-93. Please replace claims 39, 41-48, 50-56, and 74 with amended claims 39, 41-48, 50-56, and 74 as follows:

39. (Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by a sidewall region between said first and second levels; and

an ion implantation doped BST high dielectric constant thin film material formed at least on said sidewall region; the doping of said BST thin film material being such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region.

41. (Amended) The capacitor according to claim 39, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

42. (Amended) The capacitor according to claim 39, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

43. (Amended) The capacitor according to claim 39, wherein said BST high dielectric thin film material is doped with Ti.

44. (Amended) The capacitor according to claim 43, wherein said doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. (Amended) The capacitor according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. (Amended) The capacitor according to claim 39, wherein said BST high dielectric thin film material is included in a DRAM cell.

47. (Amended) The capacitor according to claim 39, wherein said BST high dielectric thin film material is formed as part of a capacitor.

48. (Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by a sidewall region between said first and second levels;

an ion implantation doped BST high dielectric constant thin film material formed at least on said sidewall region; the doping of said BST thin film material being such that the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a capping layer provided over at least a portion of said BST thin film material.

50. (Amended) The capacitor according to claim 48, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

51. (Amended) The capacitor according to claim 48, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

52. (Amended) The capacitor according to claim 48, wherein said BST high dielectric thin film material is doped with Ti.

53. (Amended) The capacitor according to claim 52, wherein said doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

54. (Amended) The capacitor according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

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55. (Amended) The capacitor according to claim 48, wherein said BST high dielectric thin film material is included in a DRAM cell.

56. (Amended) The capacitor according to claim 48, wherein said BST high dielectric thin film material is formed as part of a capacitor.

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74. (Amended) An integrated circuit capacitor device comprising:

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a material layer having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

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a first electrode provided at least on said sidewall region;

a doped BST high dielectric constant thin film material provided on said first electrode, the doping of said BST high dielectric thin film material being such that the

stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

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a second electrode provided on said BST high dielectric thin film layer.